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Tri-State Buffer with Common Data Bus

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ABSTRACT
For the recent CMOS feature sizes power dissipation becomes an overriding concerns for VLSI circuit design. We propose a novel approach named tri-state buffer with common data bus which reduces the total power & delay of elastic buffer. The paper presents a design and implementation of tri-state buffer mechanism. This design offers also the advantage of third state (High Impedance state) of tri-state buffer. The proposed elastic buffer design using tri-state buffer is implemented in Cadence tools. The obtained result shows that our design is effective in terms 20.50 % reduction in total power, 89.67% reduction in delay.
Keywords— Cadence; Static power; delay; Buffer mechanism;

I. INTRODUCTION

Networks-on-chip (NoCs) have been developed to address the communication requirements of large-scale systems enabled by semiconductor technology scaling .Past work has attributed approximately up to 40% of the power and 11% of the area of the overall chip to the NoC. Elastic buffer using D flip-flop using master and slave latches. By adding control logic to drive the latch enable pins independently, each latch can be used as an independent storage location. Thus, the Flip-flop becomes an Elastic Buffer, a First-In-First-Out with two storage locations. This is illustrated in Figure. Elastic Buffer channels use many such EBs to form a distributed FIFO[1]. FIFO storage can be increased by adding latches to EBs or by using repeater cells for storage [15]. EBs use a ready-valid handshake to advance a flit (flow-control digit). An upstream *ready* (R) signal indicates that the downstream EB has at least one empty storage location and can store an additional flit. A downstream *valid* (V) signal indicates that the flit currently being driven is valid. A flit advances when both the ready and valid signals between two EBs are asserted at the rising clock edge. This timing convention requires at least two storage slots per clock cycle delay to avoid creating unnecessary pipeline bubbles. The rest of this paper is organized as follows: Section 2 discusses the previous work with the basic building blocks of D flip-flop, circuit diagram of D flip-flop using 18 transistors, truth table, tri-state buffer, circuit diagram of tri-state buffer using 6 transistors, truth table as well as Elastic buffer using D flip-flop .Section 3 proposed Elastic buffer design using Tri-state buffer Section 4 presents the comparison and results with tables. Finally, sections 6 presents conclusion and discuss related work. Later some results obtained from the Cadence is attached with this paper.

II. PREVIOUS WORK

2.1 DFF Buffer

The D flip-flop is widely used. It is also known as a *data* or *delay* flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. It uses 18 MOS transistor as shown in Figure….due to using more number of transistor DFF consumes more power, static and dynamic both and also increase the propagation delay.

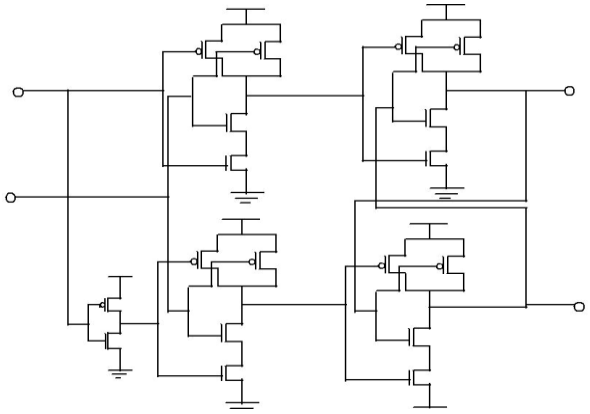

Figure 1: D Flip-Flop [2]

Table 1
Truth Table of D flip-flop

Clock	D	O(next)
Rising edge	0	0
Rising edge	1	1
Non-rising	none	Q

2.2 Tri-state buffer

Tri-state or 3-state logic allows an output port to assume a high impedance state in addition to the 0 and 1 logic levels, effectively removing the output from the circuit. This allows multiple circuits to share the same output line or lines (such as a bus).

The whole concept of the third state (Hi-Z) is to effectively remove the device's influence from the rest of the circuit. If more than one device is electrically connected, putting an output into the Hi-Z state is often used to prevent short circuits, or one device driving high (logical 1) against another device driving low (logical 0).Basically Tri-state buffer design in two part, (P1,P2) works as a inverter and (Q2, Q3) uses as a enable circuit. When enable is high data will come at the output, it may be any logic 0 or 1 and if enable is low the output will be in high impedance state. Since this buffer uses less transistor hence it consumes less power, static and dynamic both and also have reduced the propagation delay as compared to buffer using DFF.

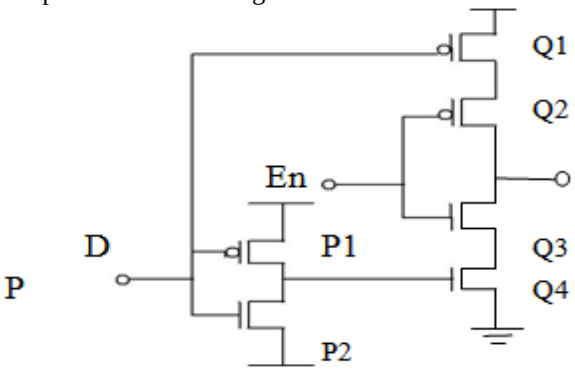

Figure 2: Tri-state Buffer [2]

3.1 Elastic buffer design using D flip-flop

As mention above when we design elastic buffer using DFF then it consume more power also more propagation delay. If we design elastic buffer using tri-state buffer then it consume less power and propagation delay also it gives the benefits of third logic of tri-state which is high impedance state of it.

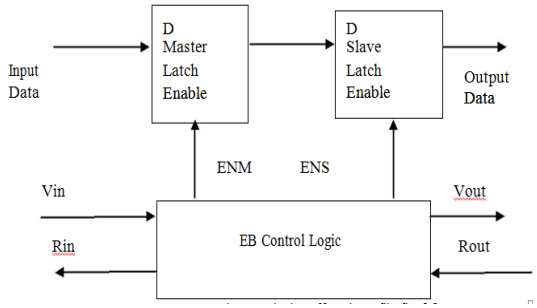

Figure 3: Elastic Buffer using D flip-flop [1]

Elastic buffer using D flip-flop using master and slave latches. By adding control logic to drive the latch enable pins independently, each latch can be used as an independent storage location. Thus, the Flip-flop becomes an Elastic Buffer, a First-In-First-Out with two storage locations. This is illustrated in Figure. Elastic Buffer channels use many such EBs to form a distributed FIFO.

III. PROPOSED WORK

The whole concept of the third state (Hi-Z) is to effectively remove the device's influence from the rest of the circuit. If more than one device is electrically connected, putting an output into the Hi-Z state is often used to prevent short circuits, or one device driving high (logical 1) against another device driving low (logical 0). When we use tri-state buffer in place of D flip-flop, the number of transistor reduced and remains only six in place of 18 transistors. Since we have use two tri-state buffer as master-slave concept hence number of transistor needed is only 12 while master-slave using D flip-flop needed 36 transistor hence area cost is reduced.

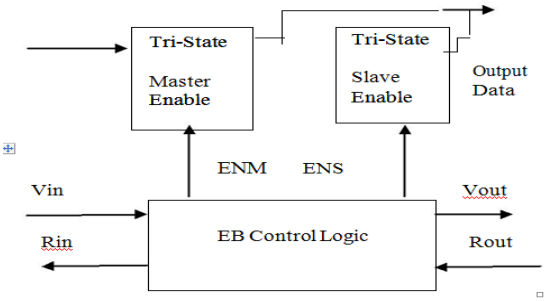

Figure 4 : Master slave tri-state buffer with control logic

Figure shows the D flip-flop is replaced by tri state buffer and whenever tri state buffer is enable it will copy the input to output and when it enable is low it goes in high state and do not copy the input into output like the D flip-flop.

Since tri-state buffer uses less transistor than D flip-flop hence result reduction in power and also reduces static and dynamic power both in some extent. When we calculate delay in D flip-flop and tri-state buffer for the same reason it also get decrease

IV. COMPARISION

4.1 Static power of elastic buffer design using D flip-flop is 14.31 mW and static power of tri-state buffer with common data bus is 11.09 mW. Hence reduction in static power of elastic buffer design using tri-state buffer is 22.50 %.

4.2 Propagation delay of D flip-flop is 21.09 ps and propagation delay in tri-state buffer is 2.177 ps. Hence reduction in propagation delay is 89.67%. Figure 5 shows the calculator window which shows the propagation delay in D flip-flop and figure 6 shows the calculator window which shows the propagation delay in Tri-state buffer.

4.3 Number of transistor used in D flip-flop is 18 and in tri-state buffer is 6 hence area cost is reduced. Figure 1 shows the number of transistor used in D flip-flop and figure 2 shows the number of transistor used in Tri-state buffer.

4.4 When D flip-flop is not enable, there is no change in output but in tri-state when it is not enable output goes in High impedance state

V. CONCLUSION

We propose a novel approach named tri-state buffer with common data bus which reduces the static power, delay and area of elastic buffer. Static power of tri-state buffer with common data bus is reduced 22.50% as compared to static power of elastic buffer design using Tri-state buffer. Propagation delay in tri-state buffer is reduced 89.67% as compared to propagation delay of D flip-flop. Number of transistor used in D flip-flop is 18 and in tri-state buffer is 6 hence area cost is reduced and provide the advantage of high impedance of tri-state buffer

References

[1] James Balfour and William J. Dally. *Design tradeoffs for tiled CMP on-chip networks*. In ICS '06: Proceedings of the 20th annual International Conference on Supercomputing, pages 187–198, 2006.

[2] Title-*CMOS VLSI Design: A Circuits and Systems Perspective*, Authors- Neil H. E. Weste, David Money Harris, Edition-4, Publisher-Addison Wesley, Length-838 pages

[3] William J. Dally. *Virtual-channel flow control*. IEEE Transaction son Parallel and Distributed Systems, 3(2):194– 205, 1992.

[4] William J. Dally and Hiromichi Aoki. *Deadlock-free adaptive routing in multicomputer networks using virtual channels*. IEEE Transactions on Parallel and Distributed Systems, 4(4):466–475, 1993.

[5] William J. Dally and Brian Towles. *Route packets, not wires: On-chip interconnection networks*. In DAC '01: roceedingsof the 38th Conference on Design Automation, pages 684–689, 2001.

[6] William J. Dally and Brian Towles. *Principles and Practices of Interconnection Networks*. Morgan Kaufmann Publishers Inc., San Francisco, CA, USA, 2003.

[7] Giovanni de Micheli and Luca Benini. *Networks on chip:A new paradigm for systems on chip design*. In DATE '02:Proceedings of the conference on Design, Automation and Test in Europe, page 418, 2002.

[8] Mike Galles. *Spider: A high-speed network interconnect*.IEEE Micro, 17(1):34–39, 1997.[9]

[9] Andreas Hansson, Kees Goossens, and Andrei R˘adulescu. *Avoiding message-dependent deadlock in network-based systems on chip*. VLSI Design, May 2007.

[10] Ron Ho, Ken Mai, and Mark Horowitz. *Efficient on-chip global interconnects*. In Symposium on VLSI Circuits, pages 271–274, 2003.

[11] John Kim, William J. Dally, and Dennis Abts. *Flattened butterfly: a cost-efficient topology for high-radix networks*. In ISCA '07: Proceedings of the 34th annual International Symposium on Computer Architecture, pages 126–137, 2007.

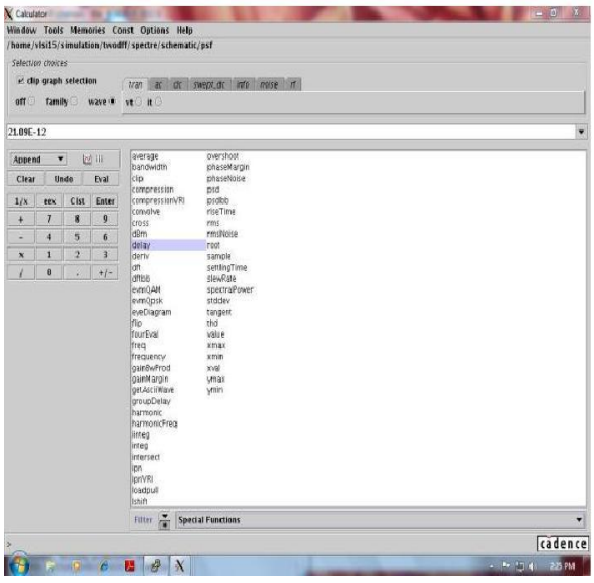

Figure 5: propagation delay in D flip-flop

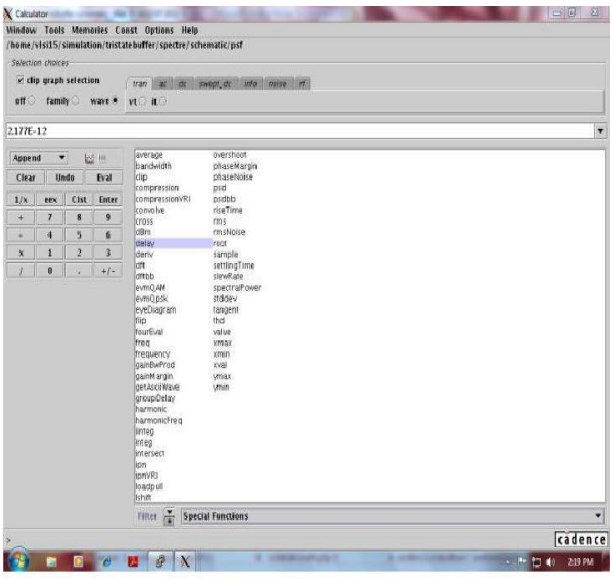

Figure 6: propagation delay in tri-state buffer